2/4 B.Tech. FIRST SEMESTER

CS3L3 **Computer Organization Lab** **Credits: 2**

(Common to CSE, IT, & ECM)

Required

Lecture: -- **Internal assessment: 25 marks**

Lab: 3 periods/week **Semester end examination: 50 marks**

Course context and Overview: A laboratory course with experiments in computer organization and interfacing techniques; digital hardware design using CAD tools and FPGAs; program-controlled and interrupt-driven I/O; memory organization; simple peripheral devices and controllers; bus interfaces; microcontroller-based designs.

Prerequisites: Computer Organization

Objectives:

1. Understanding the behavior of logic gates ,adders, decoders, multiplexers and flipflops.
2. Understanding the behavior of ALU, RAM,STACK and PROCESSOR from working modules and the modules designed by the student as part of the experiment.

Learning Outcomes:

1. Analyze the behaviour of Logic Gates with the help of HDL/ VHDL.
2. Implement sequential circuits and verify the results through simulation by VHDL.
3.Design 8-bit ALU.
4.Design 24X8 RAM.
5.Design 24X8 STACK.
6.Design 8-bit processor.

List of Experiments:

1) Introduction to Verilog HDL/VHDL

2) Verify the behavior of logic gates using truth tables(AND,OR,NOT,XOR,NAND,NOR)

3) Implementing HALF ADDER, FULL ADDER using basic logic gates

4) Implementing Binary -to -Gray, Gray -to -Binary code conversions.

5) Implementing 3-8 line DECODER.

6) Implementing 4x1 and 8x1 MULTIPLEXERS.

7) Verify the excitation tables of various FLIP-FLOPS.

8) Design of an 8-bit Input/Output system with four 8-bit Internal Registers.

9) Design of an 8-bit ARITHMETIC LOGIC UNIT.

10) Design of 2^4x8 (16 byte) RAM.

11) Design of 2^4x8 (16 byte) STACK.

12) Implementation of a 4-bit PROCESSOR.

Learning Resources

References:

1. A Verilog HDL Primer by J. Bhasker Bk&Hardcover; Published by Star Galaxy Press.
   ISBN: 0-9656277-4-8
2. Verilog HDL : A Guide to Digital Design and Synthesis by Samir Palnitkar Published by Prentice Hall Publication date: March 1996